Course Name	Course Code	semester	T + P	Credit	ECTS
Computer Organization and Architecture		5	3 + 0	3	5

Prerequisite Courses	None

Language of Course	Turkish
Course class	compulsory
Coordinator of Course	
Instructor	
Course Assistant	
Objective of Course	To computer processors and memory architectures to teach basic components for personal computer design.
Course Learning Output	Address resolution design with CISC / RISC architectures
Course Contents	An overview of computer architecture: Von Neumann - Harvard architecture, CISC and RISC architects. Instruction set design, controller and bus design, memory systems, input-output systems, interrupts, business lines, performance analysis, command formats and types of addressing.

Weeks	Topics
1	Introduction: Central Processing Unit History
2	CISC Processor; RISC Processor; ALU design;
3	Addressing keys and command structure
4	Addressing keys and command structure
5	Floating Point Numbers IEEE 754 Standard
6	Busses and Address resolution design
7	MIDTERM
8	Parallel Data Processing; Business Line (Pipeline)
9	Pipeline Problems and Solutions
10	Performance calculation; Clocks Per Instruction (CPI)
11	Input / Output Organization; Asynchronous Path Cycle; Cutting Priority Circuits
12	Memory Organization: Main memory and cache memory
13	Associated Memory
14	Memory Addressed by Content
15	FINAL EXAM

General Sufficiency
Synchronization, communication and management systems architects can be learned and used in computersystems integration to different

References
· Mano MM, Kime CR, (2001), & quot; *Logic and Computer Design Fundamentals* ", 2nd Edition, Prentice Hall .
· Hennessy JL, Patterson DA, (2003), & quot; *Computer Organization and Design: AQuantative Approach* ", 3rd Edition, Morgan Kaufmann
· Stallings W., (2006), & quot; *Computer Organization & Architecture: Designing forPerformance* ", 7th Edition Prentice Hall

Assessment
Midterm exam: 40%, Final exam: 60%; Project or homework evaluations can be made at the beginning of the semester.